

PCI Express® 2.0 Mid-Bus Probe
for Summit Analyzers
Installation and Usage Manual
Manual Version 1.0

February 2014

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1 Introduction

Teledyne LeCroy offers a wide variety of ways to connect PCI Express protocol analyzers to products under test. There are four common methods: Interposers, Specialty Probes, Mid-Bus Probes and Multi-lead Probes.

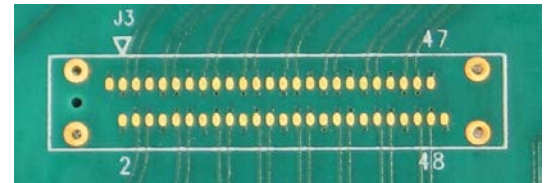
If the product uses a standard PCI Express card connector, an interposer is used which is inserted between the PCIe Card and the card slot. The interposer taps off the data traffic to allow the analyzer to monitor and record traffic with minimal perturbation of the electrical interface.

Specialty probes are used with specific card configurations, and are used in the same manner as an interposer card (in fact a specialty probe is an interposer card designed for a specific interface). LeCroy supports a range of specialty probes including ExpressCard, AMC, XMC, ExpressModule, and HP Blade Server interfaces.

If the product has an embedded PCI Express bus (e.g., a bus which runs between chips on the same circuit board), then either a mid-bus probe or a multi-lead probe can be used. The mid-bus probe requires a connection footprint (see below) to be designed into the board. The multi-lead probe allows individual connections to each bus trace on the board.

The Teledyne LeCroy mid-bus probes are 16-channel differential signal probes that meet the demand for high-density signal access, accuracy and repeatability while providing connector-less attachment to the device under test. They are based upon the configuration that was initially recommended in the Intel PCI Express Mid-Bus Probing Footprint and Pinout Revision 1.0 document dated 8/05/03 and the subsequent revisions.

A mid-bus probe is one of the tools that can greatly help engineers debugging PCI Express buses. A PCI Express mid-bus probing solution provides direct probing capability of a PCI Express bus at a width of up to 16 lanes. To accommodate a mid-bus probe, a special pad layout is required to expose the PCI Express differential pairs on the surface of the target board.



Although not part of the PCI Express specifications, the industry has developed a common mid-bus probe footprint for Gen1 and Gen2 applications as shown on the right. This footprint is recommended for use with all types of test equipment including protocol analyzers, logic analyzers and oscilloscopes. The required pad layout can be in x4 (half-size), x8 (full-size) or x16 (dual full-size) configurations depending on the maximum number of lanes that need to be probed. All footprint sizes support probing at reduced lane widths (e.g., x1) and lane widths up to the maximum footprint size. In the photo shown on page 6, the footprint occurs on the target board at "B". Note that this manual documents the mid-bus footprint used for Gen1 and Gen2 applications; the probe footprint for Gen3 is covered in the PCI Express 3.0 Mid-Bus Probe User Manual.

Teledyne LeCroy makes two versions of mid-bus probes, one for Gen1/2 (2.5 and 5 GT/s data rates) and one for Gen3 (2.5, 5 and 8 GT/s data rates). This manual covers only the Gen2 mid-bus probe. See other user manuals for the other mid-bus probes.

The Gen2 mid-bus probe is intended for use with the Summit Analyzers and is available with a half-size probe or full size probe. The half-size probe is shown on page 6. It has a two-strand ribbon cable and a connection header (B). Note that a half-size footprint supports only up to x4 lane widths.

The part numbers and components of the Teledyne LeCroy Summit T24 Gen2 mid-bus probe kit (which is also compatible with Gen1) are as follows:

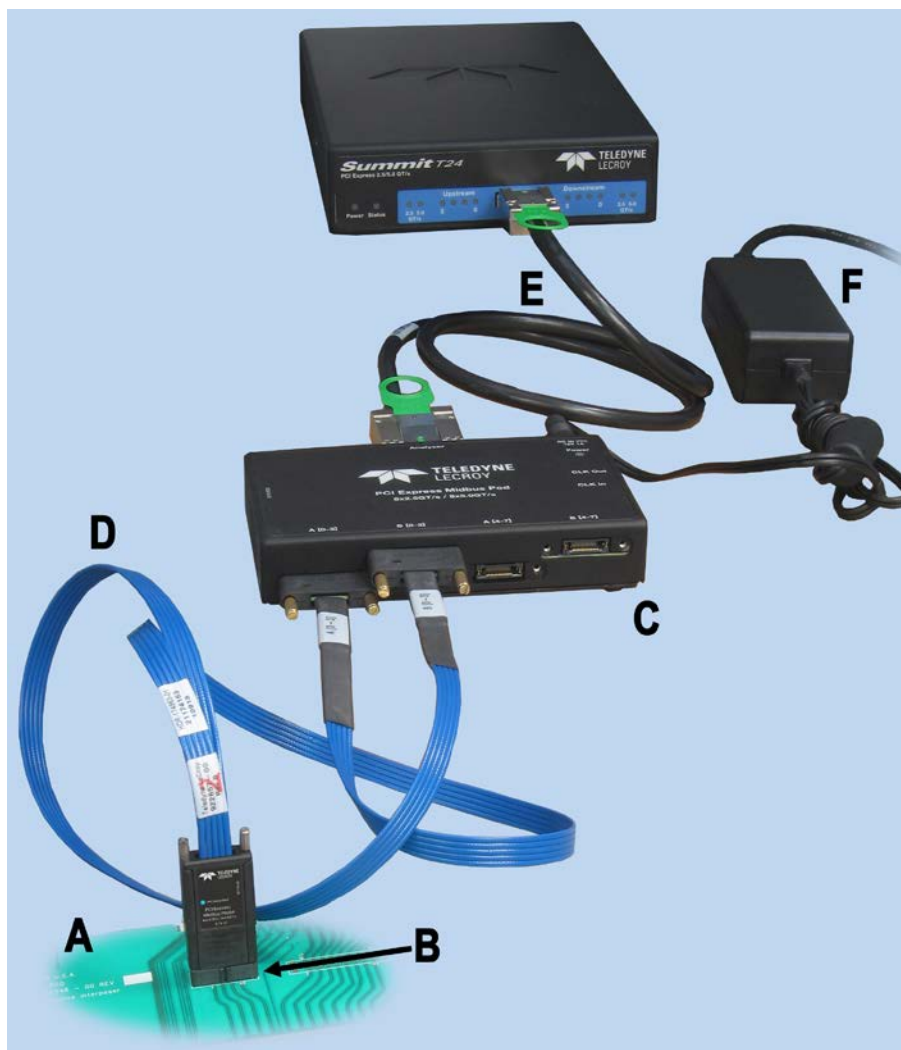
PE081ACA-X Gen2 Mid-Bus Probe, x4 Lane Width, Half-size Module, which includes:

- PE013UCA-X iPass x4 to x8 Straight Cable
- PE071UIA-X Mid-Bus Pod for Summit T24 (incl. power supply)
- PE075ACA-X Mid-bus Probe Cable (x4)
- PE014UCA-X Reference Clock Cable
- PE076ACA-X Universal Retention Module

2 Probe Components

- Universal Retention Module (B)
- Mid-Bus Probe Header Cable Assembly (D)
- Mid-Bus Probe Pod (C)
- Analyzer Cable (E)
- Power adapter for the Probe Pod (F)
- Clocking Cable Assembly (not shown)

The Intel-based mid-bus footprint specification only supplies differential lane signaling and ground reference. Should a reference clock (RefClk) be required a separate connection must be made. Teledyne LeCroy PCI Express protocol analyzers can use a reference clock probe in conjunction with the mid-bus analysis. Each mid-bus probe is equipped with one clock probe. The mid-bus reference clock probe is designed to facilitate capturing clock signals from the system board in the two configurations recommended by the Intel guideline, i.e., a tap off of an existing clock or a dedicated clock.



PCI Express target board (A) with Mid-Bus Probe (B, C and D)

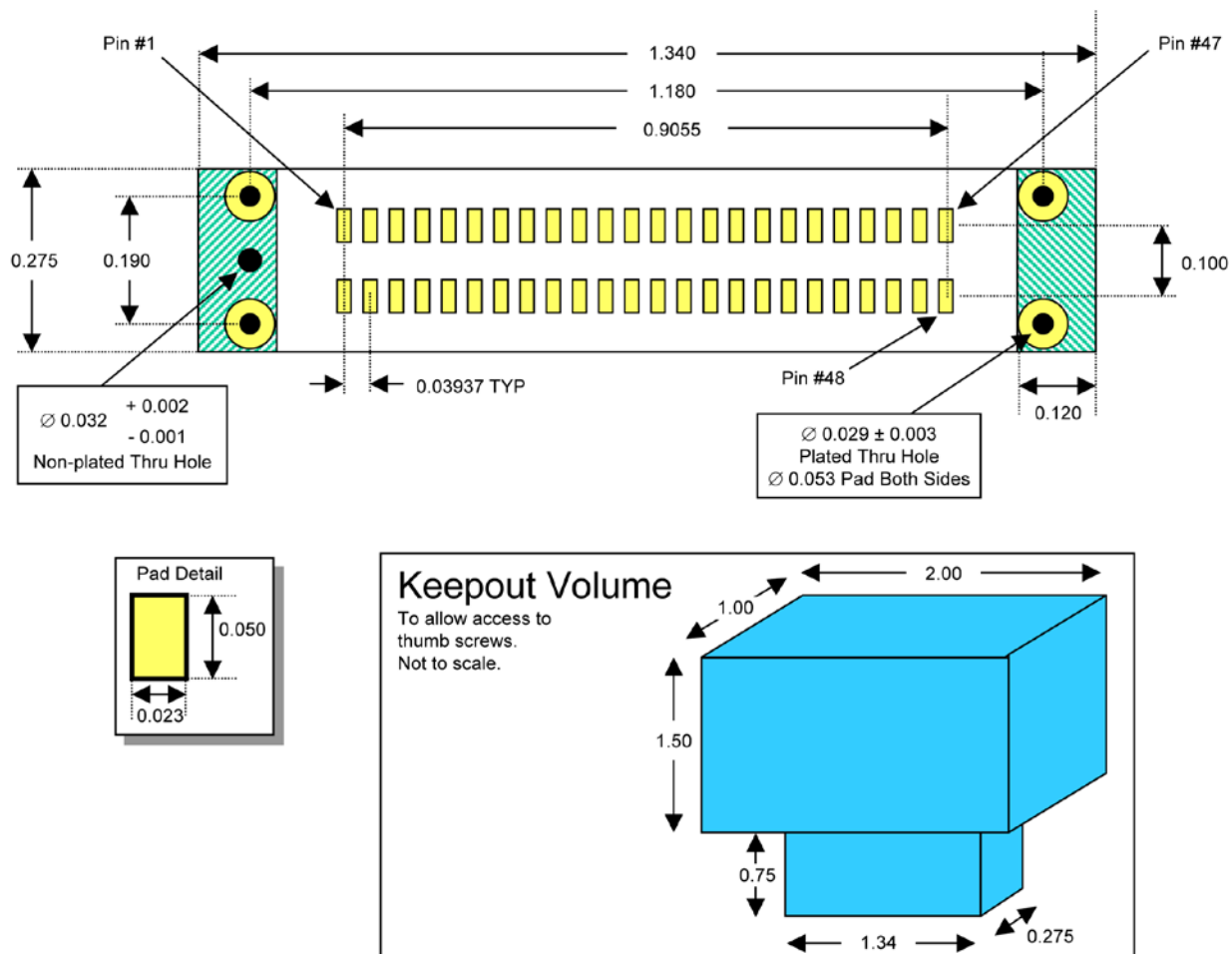
3 Mechanical Design

This section describes footprint dimensions, keepout volumes, and probe pin assignments.

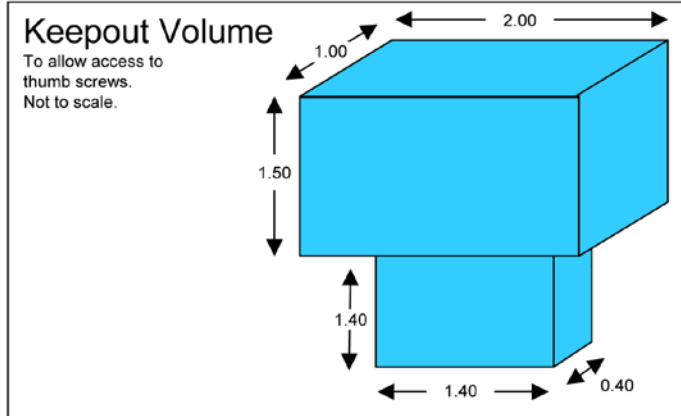
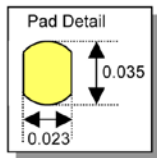
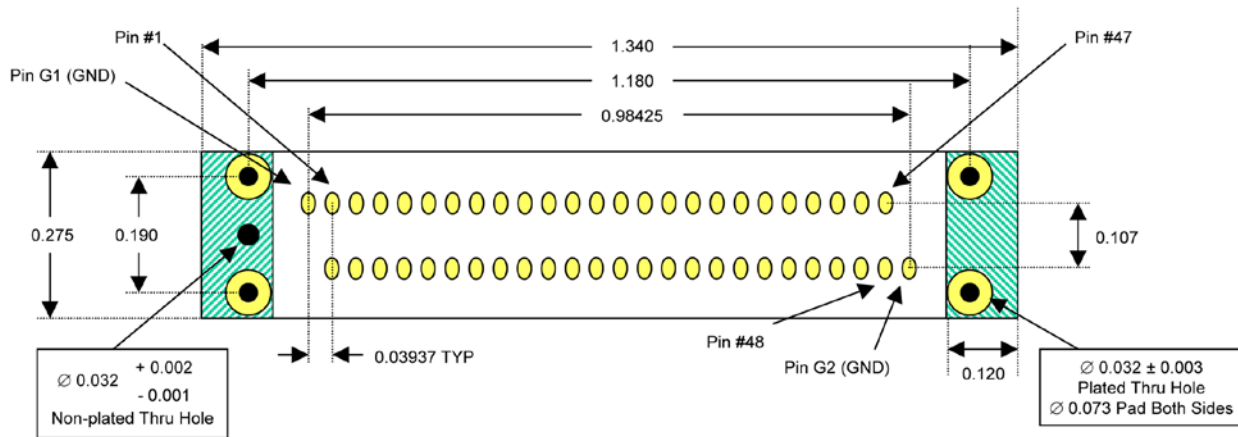
3.1 Probe Footprints

The Summit T24 Mid-bus Probe is fully compatible with the standardized mid-bus footprint recommended by the Intel guideline, as shown in the following figures.

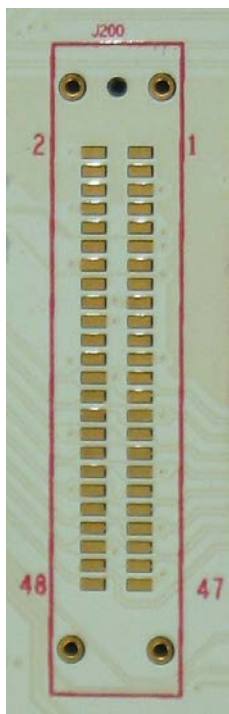
Gen1 Full-size Mid-bus Probe Footprint



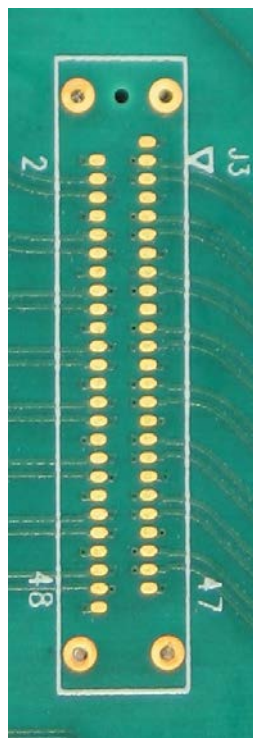
Gen2 Full-size Mid-bus Probe Footprint



A typical layout of a mid-bus footprint might look something like the following two pictures:



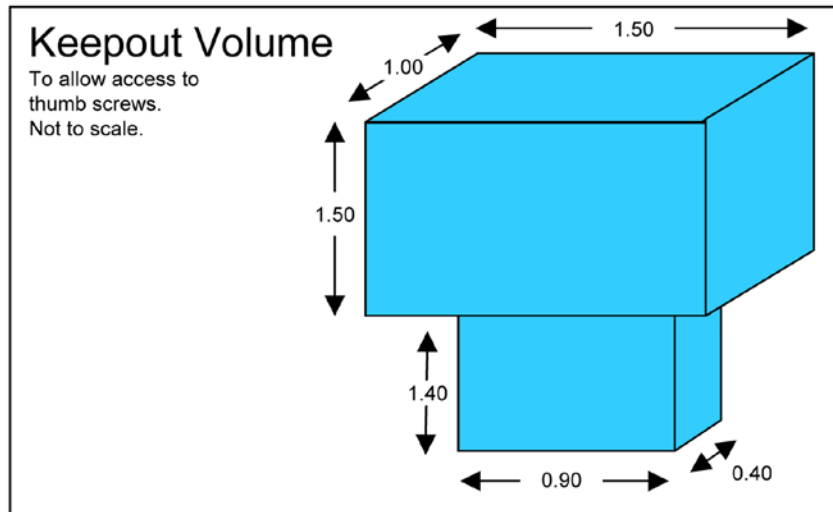
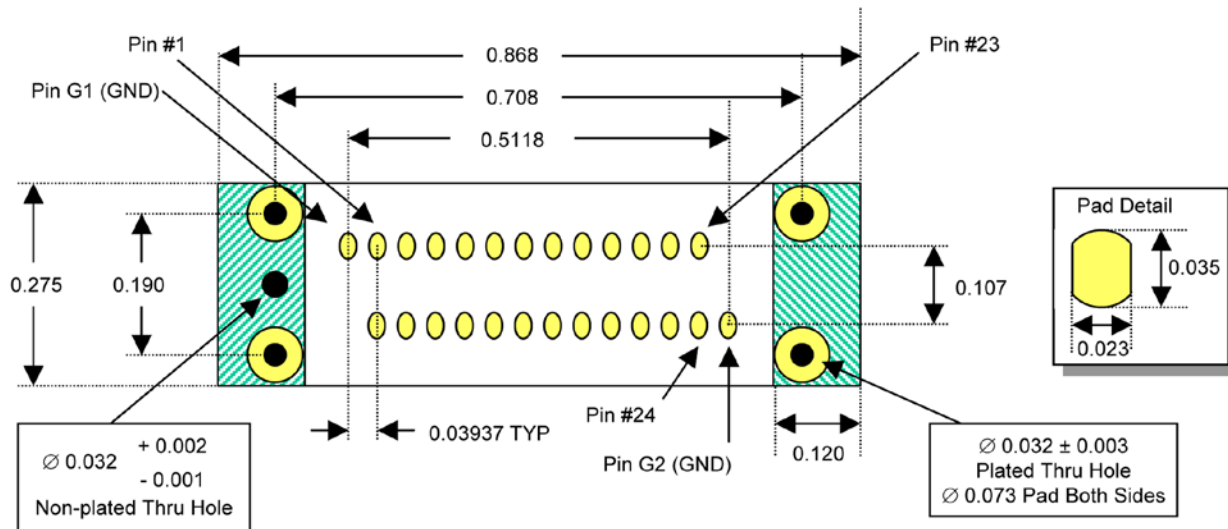
Gen1 Mid-Bus Layout



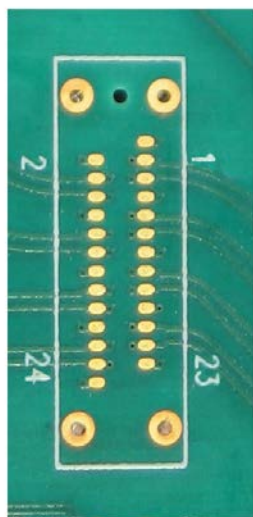
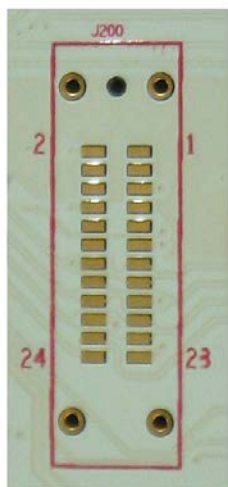
Gen2 Mid-Bus Layout

PCB Layout

Gen2 Half-size Mid-bus Probe Footprint



A typical layout of a mid-bus footprint might look something like the following two pictures:



Gen1 Mid-Bus Layout

Gen2 Mid-Bus Layout

PCB Layout

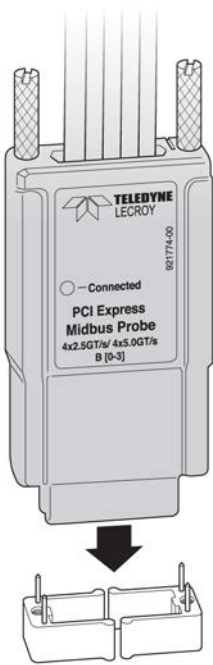
3.2 Mid-bus Probe Retention

To prepare a circuit board for PCI Express mid-bus probing, the mid-bus footprint has to be laid out onto the target system board and a retention module has to be attached to the board. Retention module attachment is simple and quick. There are four through-hole pins as part of the footprint design, two on each end of the footprint. The two holes of the Teledyne LeCroy universal retention module fit on each end of the footprint (see installation section 5). The probe aligns to the retention module with four alignment pins (two on each side), and attaches securely with thumbscrews that fasten into the retention module, holding the probe pins firmly in connection with the exposed pads of the footprint designed into the PCB.

The retention module should not be confused with a PCB connector because it is not part of the electrical circuits of either the target system or the probe. With the use of a retention module, the requirement to have a keep out area on the backside of the board is eliminated.

Retention modules can be purchased through Teledyne LeCroy:

- Half-size or full-size: P/N PE076ACA-X Universal Retention Module



3.3 Probe Connection to Analyzer

The bus signals captured by the mid-bus probe are connected to a mid-bus probe pod for amplification. This reduces the load imposed by the mid-bus probe on the target system, while allowing a longer cable to attach to the Teledyne LeCroy PCI Express protocol analyzer. The Teledyne LeCroy PCI Express protocol analyzer can then interpret these signals for full decoding and protocol analysis.

3.4 Probe Keepout Volume

As with any connection to a PCB, sufficient clearance must be allowed around the point where the probe will connect. This is defined as the keep-out volume, which must be kept clear of other components mounted on the PCB.

The probe keepout volumes are shown in the diagrams in Section 3.1.

3.5 Reference Clock Probe Attachment

Should SSC clocking be used in the system under test or if the link varies the bit rate by more than 300ppm, a reference clock tap may be required. The connection from the reference clock to the analyzer is a 3-pin header (1 by 3, 0.050" center spacing) which is placed on the clock signal transmission line of the DUT. The PE014UCA-X Reference Clock Cable provides a three-pin micro socket that connects from this header to the CLK IN port on the Mid-Bus Pod.

If the reference clock is sampled by tapping off an existing clock, the header shall be located on the existing clock transmission line, where a high impedance clock probe from the mid-bus probe is connected with no significant loading effects. In the case of a dedicated clock, the header shall be located at the end of a dedicated clock transmission line without termination, where a 50-Ohm cable is connected and the termination for the clock signal is provided on the mid-bus probe board.

The connectivity of the clock header pins follows the following table:

Signal	Pin Number
REFCLKp	1 (or 3)
Unused	2
REFCLKn	3 (or 1)

Note that the analyzer is not sensitive to the polarity of the reference clock. Therefore, the probe can be plugged onto the pin header in either orientation.

The following 3-pin header can be used for the reference clock:

Samtec Part No: TMS-103 (Vertical Orientation)

4 Electrical Design

4.1 Probe Loading Effect

The logical probing of the PCI Express bus is achieved by tapping a small amount of energy from the probed signals and channeling this energy to the analyzer. In order to avoid excessive loading conditions, the Teledyne LeCroy mid-bus probe employs high impedance tip resistors (isolation resistors). The probe isolation resistance is selected to both satisfy the probe sensitivity and system parasitic load requirements.

Extensive care has been taken to reduce the parasitic effect of the probed signals during each phase of the mid-bus probe design. An equivalent Spice model is available via the Teledyne LeCroy Protocol Systems Group support team (psgsupport@teledynelecroy.com)

With this unique design, the Teledyne LeCroy mid-bus probes can capture bus traffic signals with amplitudes specified by the PCI Express standard, while introducing only the loss and added jitter that are within the recommended specification in the PCI Express Mid-Bus Probing Footprint and Pinout.

4.2 Overview of Probe - Pin Assignments

Cross-references from the *PCI Express Mid-Bus Probing Footprint and Pinout* (8/05/03) Revision 1.0 are given in tables listed below.

In the pinout tables that follow, the following variations may be applied:

- The designation of upstream and downstream may be reversed as long as it is reversed for every lane (all upstream connections on the left and all downstream on the right may be swapped)
- Lane ordering may be reversed if done as a whole such that probe lanes 0, 1, 2, 3 connect to physical lanes 3, 2, 1, 0.
- Each differential signal pair may have the D+ and D- assignment reversed.
- If the Gen2 footprint is used, an additional ground pin is present above Pin1 and below Pin 24.

4.3 Pin Assignments for x16 Lane Widths

For x16 lane widths, two full-size headers are required. The diagrams below show the recommended pin assignments for x16 configurations (keep in mind that any of modifications mentioned in Section 4.2 can be applied, and in addition the lane swizzling feature of the Summit T3-16 and T2-16 systems noted in Section 4.2).

**x16 (in Two Unidirectional Footprints) Mid-Bus Probe Pinout
on two Full-size Headers (Summit only)**

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
A2	GND	A1	C0p- Downstream
A4	C1p- Downstream	A3	C0n- Downstream
A6	C1n- Downstream	A5	GND
A8	GND	A7	C2p- Downstream
A10	C3p- Downstream	A9	C2n- Downstream
A12	C3n- Downstream	A11	GND
A14	GND	A13	C4p- Downstream
A16	C5p- Downstream	A15	C4n- Downstream
A18	C5n- Downstream	A17	GND
A20	GND	A19	C6p- Downstream
A22	C7p- Downstream	A21	C6n- Downstream
A24	C7n- Downstream	A23	GND
A26	GND	A25	C8p- Downstream
A28	C9p- Downstream	A27	C8n- Downstream
A30	C9n- Downstream	A29	GND
A32	GND	A31	C10p- Downstream
A34	C11p- Downstream	A33	C10n- Downstream
A36	C11n- Downstream	A35	GND
A38	GND	A37	C12p- Downstream
A40	C13p- Downstream	A39	C12n- Downstream
A42	C13n- Downstream	A41	GND
A44	GND	A43	C14p- Downstream
A46	C15p- Downstream	A45	C14n- Downstream
A48	C15n- Downstream	A47	GND
G2	GND (Gen2 only)		

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
B2	GND	B1	C0p- Upstream
B4	C1p- Upstream	B3	C0n- Upstream
B6	C1n- Upstream	B5	GND
B8	GND	B7	C2p- Upstream
B10	C3p- Upstream	B9	C2n- Upstream
B12	C3n- Upstream	B11	GND
B14	GND	B13	C4p- Upstream
B16	C5p- Upstream	B15	C4n- Upstream
B18	C5n- Upstream	B17	GND
B20	GND	B19	C6p- Upstream
B22	C7p- Upstream	B21	C6n- Upstream
B24	C7n- Upstream	B23	GND
B26	GND	B25	C8p- Upstream
B28	C9p- Upstream	B27	C8n- Upstream
B30	C9n- Upstream	B29	GND
B32	GND	B31	C10p- Upstream
B34	C11p- Upstream	B33	C10n- Upstream
B36	C11n- Upstream	B35	GND
B38	GND	B37	C12p- Upstream
B40	C13p- Upstream	B39	C12n- Upstream
B42	C13n- Upstream	B41	GND
B44	GND	B43	C14p- Upstream
B46	C15p- Upstream	B45	C14n- Upstream
B48	C15n- Upstream	B47	GND
G2	GND (Gen2 only)		

A unidirectional x16 configuration can be implemented using one full-size header (utilizing the pinout diagram on the right – for upstream traffic – or the diagram on the left – for downstream traffic).

**x16 (in Two Bi-directional Footprints) Mid-Bus Probe Pinout
on two Full-size Headers (Summit only)**

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
A2	GND	A1	C0p- Upstream
A4	C0p- Downstream	A3	C0n- Upstream
A6	C0n- Downstream	A5	GND
A8	GND	A7	C1p- Upstream
A10	C1p- Downstream	A9	C1n- Upstream
A12	C1n- Downstream	A11	GND
A14	GND	A13	C2p- Upstream
A16	C2p- Downstream	A15	C2n- Upstream
A18	C2n- Downstream	A17	GND
A20	GND	A19	C3p- Upstream
A22	C3p- Downstream	A21	C3n- Upstream
A24	C3n- Downstream	A23	GND
A26	GND	A25	C4p- Upstream
A28	C4p- Downstream	A27	C4n- Upstream
A30	C4n- Downstream	A29	GND
A32	GND	A31	C5p- Upstream
A34	C5p- Downstream	A33	C5n- Upstream
A36	C5n- Downstream	A35	GND
A38	GND	A37	C6p- Upstream
A40	C6p- Downstream	A39	C6n- Upstream
A42	C6n- Downstream	A41	GND
A44	GND	A43	C7p- Upstream
A46	C7p- Downstream	A45	C7n- Upstream
A48	C7n- Downstream	A47	GND
G2	GND (Gen2 only)		

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
B2	GND	B1	C8p- Upstream
B4	C8p- Downstream	B3	C8n- Upstream
B6	C8n- Downstream	B5	GND
B8	GND	B7	C9p- Upstream
B10	C9p- Downstream	B9	C9n- Upstream
B12	C9n- Downstream	B11	GND
B14	GND	B13	C10p- Upstream
B16	C10p- Downstream	B15	C10n- Upstream
B18	C10n- Downstream	B17	GND
B20	GND	B19	C11p- Upstream
B22	C11p- Downstream	B21	C11n- Upstream
B24	C11n- Downstream	B23	GND
B26	GND	B25	C12p- Upstream
B28	C12p- Downstream	B27	C12n- Upstream
B30	C12n- Downstream	B29	GND
B32	GND	B31	C13p- Upstream
B34	C13p- Downstream	B33	C13n- Upstream
B36	C13n- Downstream	B35	GND
B38	GND	B37	C14p- Upstream
B40	C14p- Downstream	B39	C14n- Upstream
B42	C14n- Downstream	B41	GND
B44	GND	B43	C15p- Upstream
B46	C15p- Downstream	B45	C15n- Upstream
B48	C15n- Downstream	B47	GND
G2	GND (Gen2 only)		

4.4 Pin Assignments for x8 Lane Widths

For x8 lane widths, one full-size header is required. The diagram below shows the recommended pin assignments for x8 configurations (keep in mind that any of modifications mentioned in Section 4.2 can be applied, and in addition the lane swizzling feature of the Summit T3-16 and T2-16 systems noted in Section 4.2).

**x8 (Bi-directional) Mid-Bus Probe Pinout
on a Full-size Header**

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND
32	GND	31	C5p- Upstream
34	C5p- Downstream	33	C5n- Upstream
36	C5n- Downstream	35	GND
38	GND	37	C6p- Upstream
40	C6p- Downstream	39	C6n- Upstream
42	C6n- Downstream	41	GND
44	GND	43	C7p- Upstream
46	C7p- Downstream	45	C7n- Upstream
48	C7n- Downstream	47	GND
G2	GND (Gen2 only)		

4.5 Pin Assignments for x4 Lane Widths

For x4 lane widths, a half-size header can be used. The diagram below shows the recommended pin assignments for x4 configurations (keep in mind that any of modifications mentioned in Section 4.2 can be applied).

x4 (Bi-directional) Mid-Bus Probe Pinout on a Half-size Header

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
G2	GND (Gen2 only)		

4.6 Pin Assignments for x2 Lane Widths

For x2 lane widths, a half-size header can be used. The diagram below shows the recommended pin assignments for x2 configurations.

x2 (Bi-directional) Mid-Bus Probe Pinout on a Half-size Header

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND
G2	GND (Gen2 only)		

4.7 Pin Assignments for x1 Lane Widths

For x1 lane widths, a half-size header can be used. The diagram below shows the recommended pin assignments for x1 configurations.

x1 (Bi-directional) Mid-Bus Probe Pinout

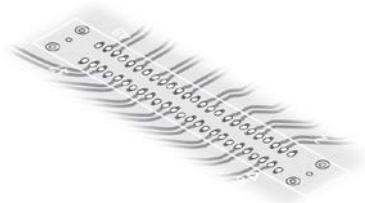
on a Full-size Header

Pin	Signal Name	Pin	Signal Name
		G1	GND (Gen2 only)
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND
G2	GND (Gen2 only)		

5 Installation of the Universal (2-piece) Gen2 Mid-bus Probe Retention Module

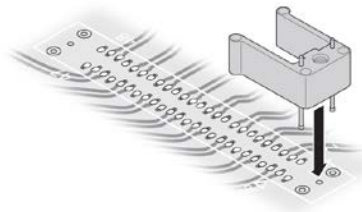
The Teledyne LeCroy Universal Retention Module is designed for use in Gen2 (or Gen1) mid-bus probe applications. The module comes in two sections, which allows the same module for either full-size or half-size mid-bus probe footprints. In this example, we will illustrate the steps to install the module, using the full-size footprint as an example. (Please note that in the illustrations, a full-size header is shown. The Gen2 Mid-bus Probe kit for the summit T24 uses a half-size header, but the steps for installation are the same).

1. Ensure that the probe footprint on the target PCB is clean and free from obstructions.

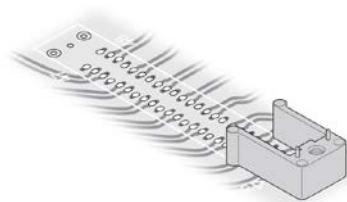


2. Align one of the pair of identical module ends into the pin hole at one end of the probe footprint.

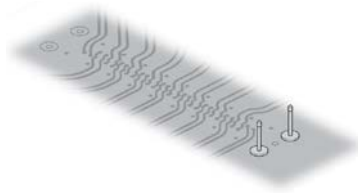
Note that the module end has two sets of pins: the short pins should face out, and the longer pins are inserted into the PCB.



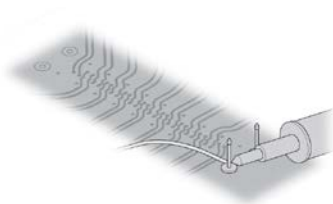
3. Insert the module end into the PCB.



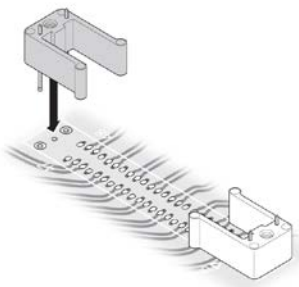
4. Turn the board over to ensure that the pins from the module end are visible and accessible on the bottom surface of the board. Note: the pins of the Universal Gen2 Retention Module are intended to accommodate PCB thicknesses up to 125 mils (3.175 mm).



5. With the module held firmly against the front surface of the board, solder the two pins into position, allowing solder to wick down into the solder hole. When the solder has set, trim the excess length of the pin flush with the board surface.



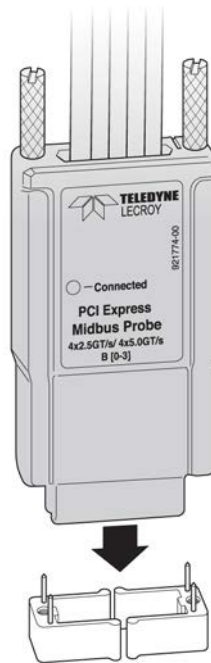
6. Turn the board right-side up, and align and insert the second module end into the opposite end of the footprint.



7. Repeat steps 4 and 5 for soldering the second module end.

5.1 Attaching the Probe head to the Retention Module

The probe design is not keyed, to allow probing of different mid-bus signal assignments. The probe head has labels indicating side A (Upstream) and side B (Downstream). Side B also has an LED indicator to show connection. Side A must face odd numbered pins (1,3,5...) and side B must face even numbered pins (2,4,6...)



1. Insert the probe head into the retention module and carefully tighten the two thumbscrews. The thumbscrews should be screwed in only finger-tight.

Caution: The probe is delicate equipment. Please tighten the thumbscrew carefully while watching the LEDs on the probe pod. Over-tightening the probe header might damage the miniature probing spring pins.

2. Connect the other side of the probe cable to the mid-bus probe pod ports marked A [0-3] and B [0-3]. The mid-bus probe pod amplifies the signal and sends it to the analyzer. The PCIe 2.0 (Gen2) probe pod is shown on next page.

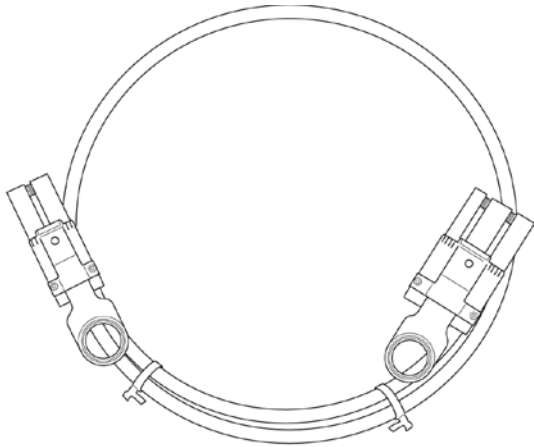


3. If you intend to use the analyzer's reference clock, connect the three pin clock cable to the port marked "CLK In" (Reference Clock In) on the mid-bus probe pod. Connect the other end of the clock cable to the three-pin reference clock header on the PCI Express board. Orientation of the cable does not matter.
4. Connect the wider end iPass x4 to x8 analyzer cable to the pod port marked "Analyzer." Connect the other side of the cable to the Summit T24 analyzer.

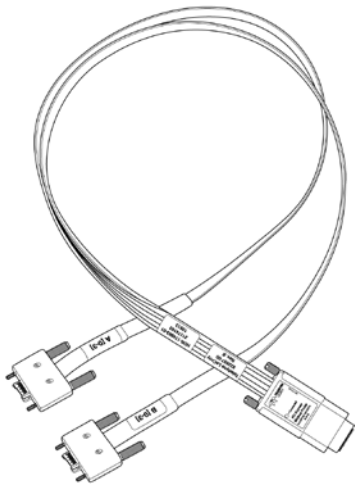
5.2 Cables

The following cables are used .

5.2.1 iPass x4 to x8 Straight Cable



5.2.2 Half-size Gen2 Mid-bus Probe Cable and Header Assembly



5.2.3 Reference Clock Cable

The Reference Clock Cable (PE014UCA-X) connects the Mid-Bus Pod to the DUT so that the pod can use the clock from the DUT. The cable has a 3-pin micro socket at one end that attaches to a 3-pin header (0.050" spacing) designed into the DUT, and the other end connects to the **Clk In** port on the Mid-Bus Probe Pod.



5.2.4 Daisy Chain Cable

The Daisy Chain Cable (PE009UCA-X) connects multiple Mid-Bus Pods together so they can share the same clock. One end of the connector is attached to the **Clk Out** port of the Mid-Bus Pod supplying the clock signal, and the other end is connected to the **Clk In** port of the other Mid-Bus Pod.

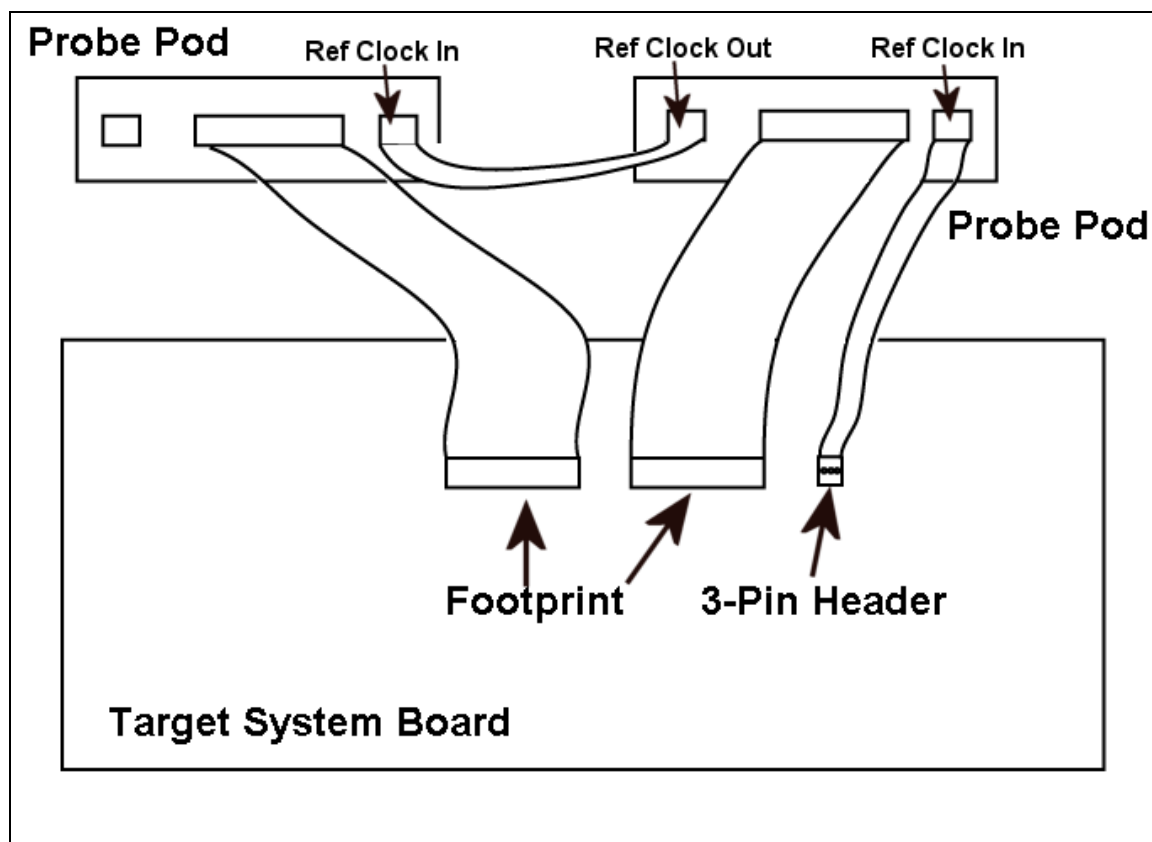


6 Dual Probe Pod Setup Using External Clocking

The steps outlined above describe a single Probe/single analyzer configuration. In a dual analyzer setup, a second probe may need to be added depending on the type of link that is being recorded.

If the analyzer internal clock is to be used, then cable the target device to the probe pod as follows - however, omit the 3-pin reference clock cable(s) shown in the illustration.

If external clocking is to be used, using the PE014UCA-X Ref Clock cable, connect the 3-pin reference clock cable from the 3-pin header on the system board to the **CLK IN** port on one probe pod. Then using the PE009UCA-X Daisy Chain Cable, connect the **CLK OUT** port on that same pod and connect it to the **CLK IN** port on the second pod. The setup is shown below.



7 Recording Traffic

Once you have set up the mid-bus probe, please note that the Break Connection button in the analyzer software does not function. This button is intended for use with the Teledyne LeCroy interposers that have link disconnect functionality (Gen1 slot interposers).



For instructions on setting up and implementing a recording, please refer to the analyzer user manual.

8 Ordering Information

Use the following table of part numbers and descriptions to order components of the Mid-bus probes.

Gen2 Analyzer Mid-bus Probes	
PE082UIA-X	Mid-bus Pod –one (1) G2 Mid-bus pod and one (1) power supply
PE081ACA-X	Gen2 Half-size Mid-Bus Probe Kit includes one (1) Gen2 Mid-Bus Pod, one (1) iPass x4-to-x8 straight cable, one (1) Ref Clock Cable, one (1) Half-size Mid-Bus Probe cable, power supply and one (1) Universal retention module
PE075ACA-X	Gen2 Half-size Mid-Bus Probe Cable, one (1) Gen2 Half-size Probe Cable (connects to Mid-bus box)
PE076ACA-X	Universal retention module (Gen1 or Gen2) 1 piece (2 halves)
PE013UCA-X	x4-to-x8 Straight iPass Cable (for Summit T24, T2-16, T28, T3-8 or T3-16), 1 meter
PE014UCA-X	Reference Clock Cable (for use with x4 Multi-lead Pod and Mid-bus Pod)

Appendix A

How to Contact Teledyne LeCroy

Type of Service	Contact
Call for technical support...	PSG Support Hotline 1-408-653-1260
Fax your questions...	Worldwide: 1 (408) 727-6622
Write a letter ...	Teledyne LeCroy Customer Support 3385 Scott Blvd. Santa Clara, CA 95054
Send e-mail...	psgsupport@teledynelecroy.com
Visit Teledyne LeCroy's web site...	teledynelecroy.com/